

# Design and Technology of AlGaAs/GaAs HBT for High Temperature Circuits

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## Abstract

In the last years HBT with strongly improved performance for application at room temperature [1, 2] have been demonstrated. However, the technology for high temperature devices and circuits must be adopted. The layer design and the technology of AlGaAs/GaAs HBT for high-temperature circuits up to 623 K is presented in this paper. As a possible application of these devices an operational amplifier circuit is fabricated and measured up to 473 K.

## Introduction

Certain applications in the fields of industrial process control, space activities, automotive [3] -and aircraft industries require devices which may operate up to 700 K. For reliable operation at this elevated temperatures not only the material system, but also the technology used for fabrication has to be adapted.

The GaAs material-system with its high bandgap of 1.4eV and its high maturity, achieved in the recent years, is a very interesting candidate for high temperature circuits [4]. Related to the material, the choice of technology is a very important point. Temperature enhanced degradation effects, for example in ohmic contacts, could degrade high temperature performance. But also the device simulation in combination with circuit design has to be adapted in order to extend the operation range beyond the usual military range.

Therefore the effort of high temperature circuitry needs a comprehensive consideration of several influencing factors.

## High-Temperature HBT Wafer Design

In Fig. 1 the two wafer structures, for a single-HBT (SHBT) and a double-HBT (DHBT) are shown. SHBT and DHBT have high Al mole fractions of 45% and 42% in the emitter to suppress the hole diffusion from base into the emitter even at high temperatures yielding a sufficient current gain for this temperatures.

In order to suppress the thermal generated electron-hole current from the space charge region of the base-collector diode into the base, an Al mole fraction of 20% was employed in the collector of the DHBT. This leakage current is linear proportional to the intrinsic carrier density in the collector layer.

Since AlGaAs has a significantly lower intrinsic carrier density than GaAs this thermal generated current is also lower. Additionally AlGaAs has a higher bandgap and lower ionization coefficients than GaAs. Therefore the breakdown voltage of the base collector junction in the DHBT is significantly higher than in the SHBT.

In Fig. 2 the common emitter output characteristics of a fabricated SHBT and a DHBT are shown, demonstrating the superior properties of the double heterostructure. From 573K the SHBT suffers from the thermal induced base-collector junction leakage current in contrast to the DHBT which shows up to 623K a low output conductance.

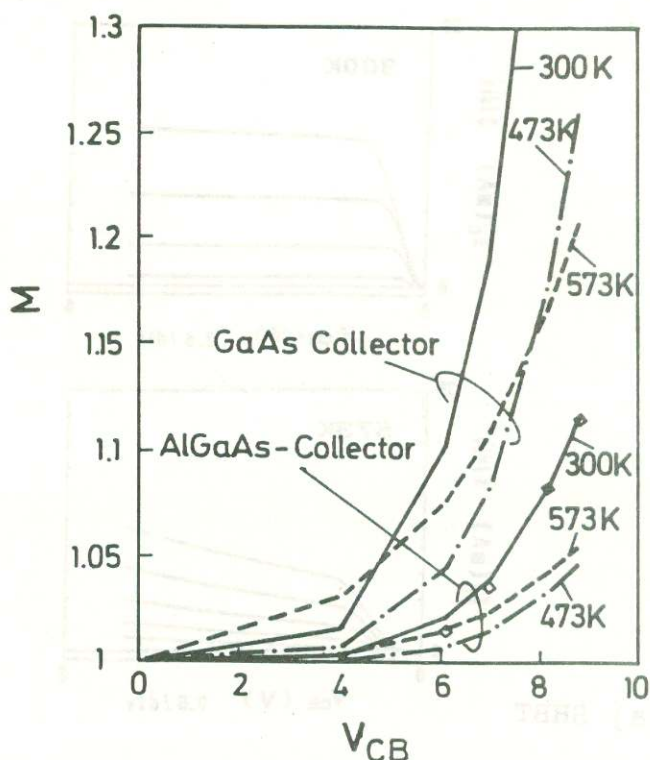


Figure 3: Temperature dependence of multiplication factor  $M$  for a GaAs and an  $Al_{0.2}Ga_{0.8}As$  collector.

The results in Fig. 3 illustrate the differences in the breakdown behaviour of the two device structures. The carrier multiplication factor  $M$ , which is the ratio of the electron currents leaving and entering the base collector space charge region, is influenced by avalanche multiplication and thermal generation of charge carriers.



	SHBT			DHBT		
	Doping Concentration ( $\text{cm}^{-3}$ )	Thick-ness (nm)	Al-mole fraction (%)	Doping Concentration ( $\text{cm}^{-3}$ )	Thick-ness (nm)	Al-mole fraction (%)
Emitter	$1 \cdot 10^{18}$ (Si)	100	0	$5 \cdot 10^{18}$ (Si)	150	0
	$4 \cdot 10^{17}$ (Si)	50	0-45	$4 \cdot 10^{17}$ (Si)	500	0
		150	45		20	0-42
		50	45-0		30	42
	undoped	10	0			
Base	$8 \cdot 10^{18}$ (Zn)	150	0	$2 \cdot 10^{19}$ (C)	100	0
Collector					30	0-20
	$4 \cdot 10^{16}$ (Si)	500	0	$4 \cdot 10^{16}$ (Si)	500	20
	$1 \cdot 10^{18}$ (Si)	500	0	$5 \cdot 10^{18}$ (Si)	500	0

Figure 1: Wafer structure of fabricated high temperature SHBT and DHBT.

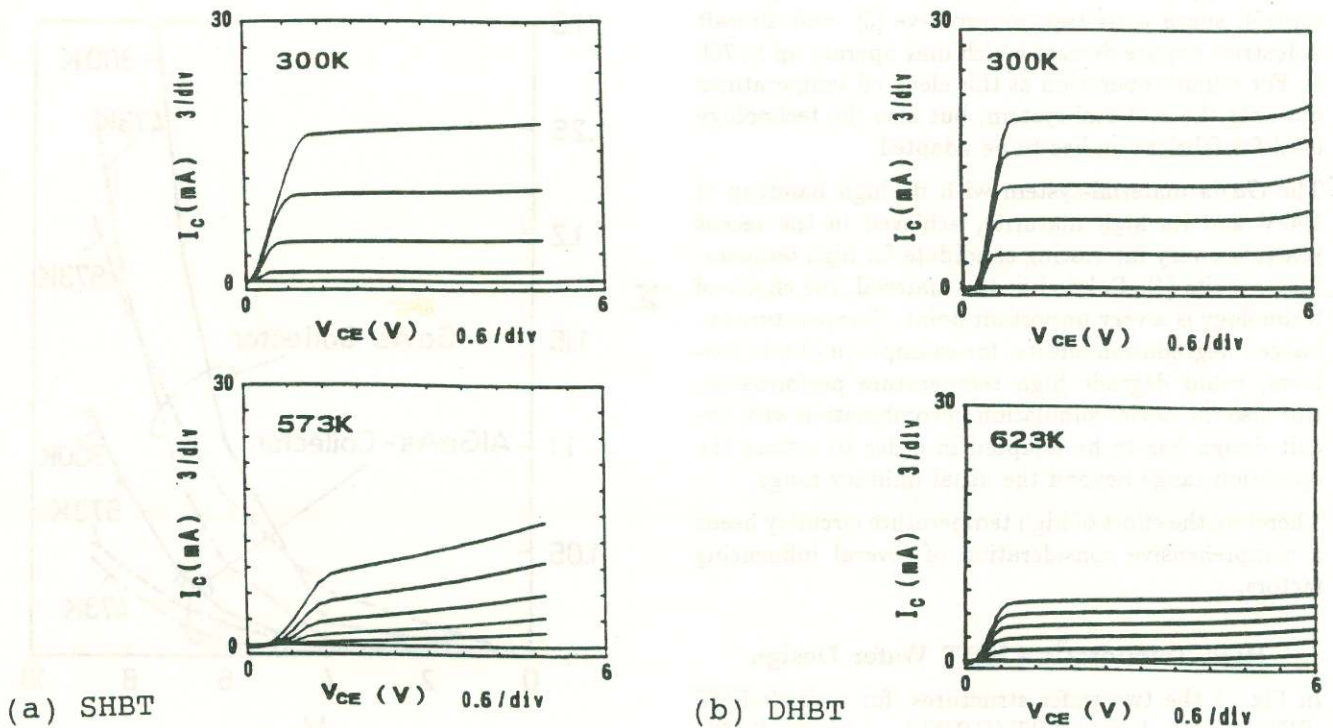


Figure 2: Common emitter output characteristics of fabricated high temperature SHBT and DHBT for various temperatures.



ers. The simulation has been performed for a transistor with  $40\mu\text{m} \times 65\mu\text{m}$  base-collector junction area with a collector doping of  $6 \cdot 10^{16}\text{cm}^{-3}$  and a sub-collector doping level of  $5 \cdot 10^{18}\text{cm}^{-3}$ . The collector thickness is  $500\text{nm}$ . The simulation shows clearly [5], [6], that the avalanche breakdown voltage has a negative temperature coefficient. The increase in multiplication factor for higher temperatures is because of thermal generated charge carriers in the space charge region.

### Device and Circuit Technology

Essential for the realization of reliable devices are the stability of the ohmic contacts and the surface passivation. For the high-temperature stable n-ohmic contacts  $\text{Ni}/\text{Ge}/\text{Ni}/\text{Au}$  and  $\text{Pd}/\text{S}/\text{In}/\text{Pd}$  [7, 8] metallization systems were used.  $\text{WSi}$ ,  $\text{W}$  and  $\text{LaB}_6$  [9] were employed as a diffusion barrier between the active ohmic contact layer and the Au metallization. For p-type ohmic base contacts  $\text{Ti}/\text{Pt}/\text{Au}$  is generally used.

PECVD deposited  $\text{SiN}$  is employed for device-passivation. The passivation is optimized for the high-temperature requirements such as to prevent the out-diffusion of As atoms at elevated temperatures, stabilize against surface degradation. The passivation therefore effectively suppresses surface leakage currents.

The substrate between the transistors is covered with an evaporated  $\text{Al}_x\text{O}_y$  layer with a thickness of about  $500\text{nm}$ . This layer with its excellent insulating properties over the whole operating temperature range ensures a very good adhesion between the plated bonding pads the  $\text{Al}_x\text{O}_y$  layer, and the semi-insulating substrate.

The interconnection-metallization is generally placed on the  $\text{Al}_x\text{O}_y$  layer. An air-bridge technique is used to connect the individual transistors with this metallization.

In high-temperature circuits flash-evaporated  $\text{NiCr}$  metall-films are utilized for resistors, because of the low temperature coefficient of  $\text{NiCr}$  and the possibility to control the value of evaporated resistivity in situ. The resistors are embedded between the  $\text{Al}_x\text{O}_y$  layer and the  $\text{SiN}$  layer.

For low frequency applications triple mesa HBTs and for high frequency performance self-aligned HBTs according to Fig. 4 have been fabricated. For both devices the emitter-mesa is defined by a  $\text{H}_2\text{O}_2 : \text{NH}_4\text{OH} = 100 : 0.6$  solution, which etches GaAs selectively to AlGaAs. Immediately before the evaporation of the base contacts the AlGaAs layer is removed with  $\text{H}_2\text{O}_2 : \text{NH}_4\text{OH} : \text{H}_2\text{O} = 2 : 6 : 300$ . For the formation of the base mesa and the device isolation an etchant consisting of  $\text{H}_3\text{PO}_4 : \text{H}_2\text{O}_2 : \text{Methanol} = 14 : 8 : 42$  is used.

The self-aligned structure is related to relatively small device dimensions in comparison with the triple mesa structure. This is not only a prerequisite for high frequency devices but also an advantage for high tempe-

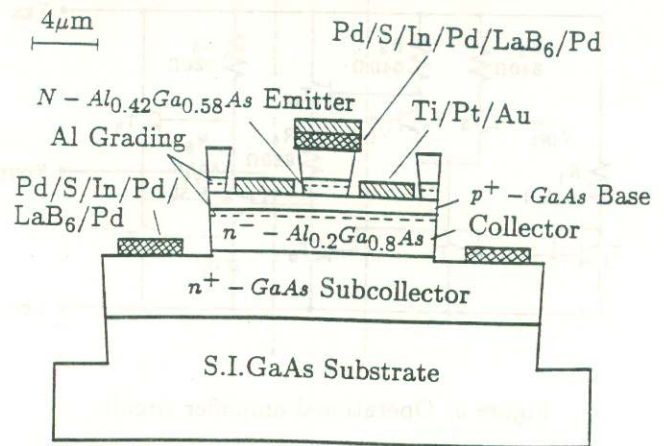


Figure 4: Cross section of a self-aligned DHBT.

perature devices. The already mentioned base-collector junction leakage current depends linearly on the volume of the space charge region of this junction. Therefore a small device will have superior output characteristics in comparison to a relatively large device at high temperatures.

### Circuit Design

The circuit design is performed with Aim-Spice. The implemented HBT model, based on gummel-poon equations [10], is not suitable for high temperature circuit simulation, because it does not support the temperature dependence of ideality factors, it does not consider thermal generated leakage currents, and does not take under consideration the influence of heterojunctions in a HBT on device performance. Therefore a physical based model has been developed and implemented into Aim-Spice [11]. The following features have been introduced into the model: thermionic emission and tunneling at the emitter-base junctions, rigorous correction of the depletion depth at large forward bias at both junctions, impact ionization at the base collector junction, field dependent emitter and collector resistances at high current levels, current spreading and emitter crowding. With this program also the simulation of high-temperature and high-frequency performance of circuits is possible.

### Circuit

As an example for circuits operating at high ambient temperatures an operational amplifier has been designed and fabricated. The specifications were made according to the requirements of high temperature operating sensors with the aim of integration to a typical GaAs based sensor element with the operational amplifier.

As shown in Fig. 5 the circuit consists of three parts: input stage, level shifter, and output stage. The gain of the three amplifier stages and the resulting open



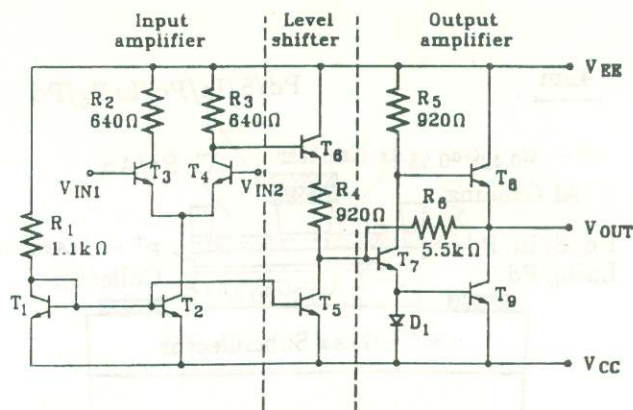


Figure 5: Operational amplifier circuit.

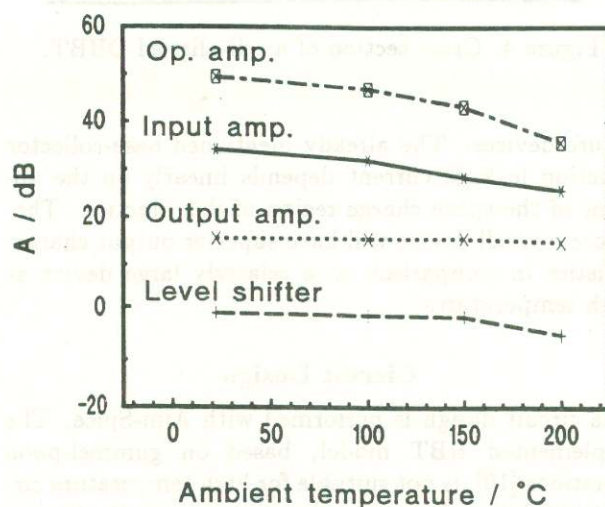


Figure 6: Open loop gain of the operational amplifier and the three amplifier stages versus temperature.

loop gain of the whole amplifier is given in Fig. 6. An operation of the circuit is possible up to 473 K. The open loop gain decreases from 49.5 dB at room temperature to 35.8 dB at 473 K. For higher temperatures circuit operation was impossible because of unpleasant changes in transistor bias currents and voltages. An improved re-design circuit is now in fabrication.

### Conclusions

This paper describes a proposal for a high temperature stable technology based on *AlGaAs/GaAs* SHBT and *AlGaAs/GaAs/AlGaAs* DHBT. The wafer design for the transistors is discussed with particular respect to temperature induced breakdown of the base collector junction. Fabrication steps for individual transistor and complete circuits are described. Important aspects of transistor and circuit simulation are pointed out. As an example an operational amplifier circuit is shown.

### Acknowledgment

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